Terms used:
segment or **partition** or **section** **sentence** **cache** or **buffer** or **register** and **miss** or **miscache** **near/6** and **least** r

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1 RAID: high-performance, reliable secondary storage

Peter M. Chen, Edward K. Lee, Garth A. Gibson, Randy H. Katz, David A. Patterson
June 1994 **ACM Computing Surveys (CSUR)**, Volume 26 Issue 2

Publisher: ACM Press

Full text available: pdf(3.60 MB) Additional Information: full citation, abstr

Disk arrays were proposed in the 1980s as a way to use parallelism between multiple disks to ir major computer manufacturers. This article gives a comprehensive overview of disk arrays and introduces disk technology and reviews the driving forces that have popularized disk arrays: pe

Keywords: RAID, disk array, parallel I/O, redundancy, storage, striping

2 Let caches decay: reducing leakage energy via exploitation of cache generational behavic

Zhigang Hu, Stefanos Kaxiras, Margaret Martonosi
May 2002 **ACM Transactions on Computer Systems (TOCS)**, Volume 20 Issue 2

Publisher: ACM Press

Full text available: pdf(873.03 KB) Additional Information: full citation, abstr

Power dissipation is increasingly important in CPUs ranging from those intended for mobile use, of the power dissipated is dynamic switching power, leakage power is also beginning to be a cor chip power will increase significantly. This article examines methods for reducing leakage power

Keywords: Cache memories, cache decay, generational behavior, leakage power

3 Data prefetch mechanisms

Steven P. Vanderwiel, David J. Lilja
June 2000 **ACM Computing Surveys (CSUR)**, Volume 32 Issue 2

Publisher: ACM Press

Full text available: pdf(172.07 KB) Additional Information: full citation, abstr

The expanding gap between microprocessor and DRAM performance has necessitated the use o memory access. Although large cache hierarchies have proven to be effective in reducing this la spend more than half their run times stalled on memory requests. Data prefetching has been pr

Keywords: memory latency, prefetching

4 eNVy: a non-volatile, main memory storage system

Michael Wu, Willy Zwaenepoel
November 1994 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proc programming languages and operating systems ASPLOS-VI**, Volume 29 ,
Publisher: ACM Press
Full text available: pdf(1.32 MB) Additional Information: full citation, abstr

This paper describes the architecture of eNVy, a large non-volatile main memory storage systen memory mapped array rather than as an emulated disk in order to provide an efficient and easy memory access times at a lower cost than other solid-state technologies. However, they have a

5 Pen computing: a technology overview and a vision

André Meyer
July 1995 **ACM SIGCHI Bulletin**, Volume 27 Issue 3
Publisher: ACM Press
Full text available: pdf(5.14 MB) Additional Information: full citation, abstr

This work gives an overview of a new technology that is attracting growing interest in public as in the use of a pen or pencil as the primary means of interaction between a user and a machine consequences that will be analyzed and put into context with other emerging technologies and \

6 Scalable high-speed prefix matching

Marcel Waldvogel, George Varghese, Jon Turner, Bernhard Plattner
November 2001 **ACM Transactions on Computer Systems (TOCS)**, Volume 19 Issue 4
Publisher: ACM Press
Full text available: pdf(933.02 KB) Additional Information: full citation, abstr

Finding the longest matching prefix from a database of keywords is an old problem with a numb management to computational geometry. But perhaps today's most frequent best matching pre Internet traffic volume and link speeds are rapidly increasing; at the same time, a growing user

Keywords: collision resolution, forwarding lookups, high-speed networking

7 Efficient management of memory hierarchies in embedded DRAM systems

Ashley Saulsbury, Su-Jaen Huang, Fredrik Dahlgren
May 1999 **Proceedings of the 13th international conference on Supercomputing ICS '99**
Publisher: ACM Press
Full text available: pdf(1.57 MB) Additional Information: full citation, references, citings, index terms

Keywords: COMA, DRAM, cache, latency, memory hierarchy, processor

8 Trace-driven memory simulation: a survey

Richard A. Uhlig, Trevor N. Mudge
June 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 2
Publisher: ACM Press
Full text available: pdf(636.11 KB) Additional Information: full citation, abstr

As the gap between processor and memory speeds continues to widen, methods for evaluating increasingly important. One such method, trace-driven memory simulation, has been the subjec development and substantial improvements during the past decade. This article surveys and an

Keywords: TLBs, caches, memory management, memory simulation, trace-driven simulation

9 Power reduction techniques for microprocessor systems

Vasanth Venkatachalam, Michael Franz
September 2005 **ACM Computing Surveys (CSUR)**, Volume 37 Issue 3
Publisher: ACM Press
Full text available: pdf(602.33 KB) Additional Information: full citation, abstr

Power consumption is a major factor that limits the performance of computers. We survey the " microprocessor system over time. These techniques are applied at various levels ranging from c applications. They also include holistic approaches that will become more important over the ne

Keywords: Energy dissipation, power reduction

10 Classics in software engineering

January 1979 Divisible Book
Publisher: Yourdon Press
Additional Information: full citation, cited by, index terms

11 Cache memory performance in a unix enviroment

Cedell Alexander, William Keshlear, Furrokh Cooper, Faye Briggs
June 1986 **ACM SIGARCH Computer Architecture News**, Volume 14 Issue 3
Publisher: ACM Press
Full text available: pdf(2.10 MB) Additional Information: full citation, citings, index terms

12 The *Conquest* file system: Better performance through a disk/persistent-RAM hybrid desig

An-I Andy Wang, Geoff Kuenning, Peter Reiher, Gerald Popek
August 2006 **ACM Transactions on Storage (TOS)**, Volume 2 Issue 3
Publisher: ACM Press
Full text available: pdf(1.34 MB) Additional Information: full citation, abstr

Modern file systems assume the use of disk, a system-wide performance bottleneck for over a c access memory content or fail to provide mechanisms to achieve data persistence across reboot inexpensive, which enables all file system services to be delivered from memory, except for pro

***Keywords**: Persistent RAM, file systems, performance measurement, storage management*

13 UTLB: a mechanism for address translation on network interfaces

Yuqun Chen, Angelos Bilas, Stefanos N. Damianakis, Cezary Dubnicki, Kai Li
October 1998 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proc programming languages and operating systems ASPLOS-VIII**, Volume 3
Publisher: ACM Press
Full text available: pdf(1.76 MB) Additional Information: full citation, abstr

An important aspect of a high-speed network system is the ability to transfer data directly betw network interface to "know" the virtual-to-physical address translation of a user buffer, *i.e.*, the translation architecture, User-managed TLB (UTLB), which eliminates system calls and device in

14 The VMP network adapter board (NAB): high-performance network communication for mu

H. Kanakia, D. Cheriton
August 1988 **ACM SIGCOMM Computer Communication Review , Symposium procee**
Issue 4
Publisher: ACM Press
Full text available: pdf(1.63 MB) Additional Information: full citation, abstr

High performance computer communication between multiprocessor nodes requires significant i adapter interfaces impose excessive processing, system bus and interrupt overhead on a multip host resources such as the system bus and the processors, or else intelligent but too slow, beca

15 Mapping irregular applications to DIVA, a PIM-based data-intensive architecture
Mary Hall, Peter Kogge, Jeff Koller, Pedro Diniz, Jacqueline Chame, Jeff Draper, Jeff LaCoss, John (Shin, Joonseok Park
January 1999 **Proceedings of the 1999 ACM/IEEE conference on Supercomputing (C**
Publisher: ACM Press
Full text available: pdf(111.41 KB) Additional Information: full citation, refere

16 Missing the memory wall: the case for processor/memory integration
Ashley Saulsbury, Fong Pong, Andreas Nowatzyk
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd**
Issue 2
Publisher: ACM Press
Full text available: pdf(1.45 MB) Additional Information: full citation, abstr

Current high performance computer systems use complex, large superscalar CPUs that interface CPU-centric designs invest a lot of power and chip area to bridge the widening gap between CPU systems and are limited by the memory subsystem performance.This paper argues for an integr

17 A taxonomy-based comparison of several distributed shared memory systems
Ming-Chit Tam, Jonathan M. Smith, David J. Farber
July 1990 **ACM SIGOPS Operating Systems Review**, Volume 24 Issue 3
Publisher: ACM Press
Full text available: pdf(1.96 MB) Additional Information: full citation, abstr

Two possible modes of Input/Output (I/O)are "sequential" and "random-access", and there is ar communication, typified in the I/O setting by magnetic tape, is typified in the communication se I/O setting by a drum or disk device, is typified in the communication setting by **shared memo**

18 Cluster communication protocols for parallel-programming systems
Kees Verstoep, Raoul A. F. Bhoedjang, Tim Rühl, Henri E. Bal, Rutger F. H. Hofman
August 2004 **ACM Transactions on Computer Systems (TOCS)**, Volume 22 Issue 3
Publisher: ACM Press
Full text available: pdf(1.29 MB) Additional Information: full citation, abstr

Clusters of workstations are a popular platform for high-performance computing. For many para performance. Several modern System Area Networks include programmable network interfaces by the host processors. Finding the right trade-off between protocol processing at the host and

Keywords: Clusters, parallel-programming systems, system area networks

19 Processor-memory coexploration using an architecture description language
Prabhat Mishra, Mahesh Mamidipaka, Nikil Dutt
February 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Is
Publisher: ACM Press

Full text available: pdf(201.88 KB) Additional Information: full citation, abstr

Memory represents a major bottleneck in modern embedded systems in terms of cost, power, a systems assume a fixed cache hierarchy. With the widening processor--memory gap, more aggr of a heterogeneous memory architecture tuned for specific target applications. However, such a

Keywords: Processor--memory codesign, architecture description language, design space expl

20 A survey of commercial parallel processors

Edward Gehringer, Janne Abullarade, Michael H. Gulyn
September 1988 **ACM SIGARCH Computer Architecture News**, Volume 16 Issue 4
Publisher: ACM Press
Full text available: pdf(2.96 MB) Additional Information: full citation, abstr

This paper compares eight commercial parallel processors along several dimensions. The proces Balance system, the Alliant FX series, and the ELXSI System 6400) and four network multiproce paper contrasts the computers from the standpoint of interconnection structures, memory confi

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	10616	(plurality or multiple) adj2 bank$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/22 13:26
L2	9183	first adj2 bank$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/22 13:26
L3	8127	second adj2 bank$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/22 13:26
L4	425	size near3 ("same" or equal$4) near5 bank$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/22 13:26
L5	1760	L1 and L2 and L3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/22 13:26
L6	56	L5 and L4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/22 13:26
L7	101922	interleav$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/22 13:26
L8	19	L6 and L7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/22 13:26
L9	25500983	@ad<"20040211"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/22 13:26

EAST Search History

L10	19	L8 and L9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/22 13:26
L11	862558	segment$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/22 13:26
L12	6	L10 and L11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/22 13:26